2.7 A 1V 2.3μW Biomedical Signal Acquisition IC

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Many patients can benefit from wearable medical devices that provide real-time monitoring and possibly on-site treatment. It is desirable for such devices to operate under a single micro battery that is light-weight and low-volume. Devices under such a constraint require operating at low supply voltage (1~1.5V) with ultra low power consumption for long battery lifetime. In addition, in order to pick up very weak biomedical signals, the device also needs to exhibit extremely low input referred noise. All of these pose a great challenge to circuit designers. This paper presents a 1V 2.3μW biomedical signal acquisition IC, as shown in Fig. 2.7.1, which consists of a low noise instrumentation amplifier with DC rejection, an 11b successive approximation ADC, and other auxiliary circuits.

Since low-noise and low-power performance are simultaneously required, an optimum trade-off between noise and current consumption is crucial. The noise-efficiency factor (NEF) [1] measures the quality of this trade-off. An ideal bipolar single-transistor amplifier has an NEF of 1.0. All practical circuits have higher NEF. Lower NEF indicates better trade-off. To achieve low NEF, the noise contribution of the input transistors should be dominant. In a typical OTA with differential input stage, this means the aspect ratio of the output transistors should be made much smaller than that of the input transistors [2]. However, at a given bias current, choosing low aspect ratios for the output transistors will lead to high overdrive voltages which prevent the output from swinging rail-rail. Thus a trade-off between noise and voltage headroom is required at the output stage. Although the noise from the output stage can also be reduced by increasing the g_m of the input transistors, the transconductance cannot be arbitrarily increased under a given bias current. To overcome this problem, a low-voltage low-power low-noise OTA (LN-OTA) is proposed and shown in Fig. 2.7.2. M1~M10 and R_i form a negative feedback loop which adjusts the gate voltages of M3 and M4 so that i_4-i_3=$2V_{in}/R_i$. It is effectively a g_m cell whose overall G_m is equal to $2/R_i$. The output of this g_m cell is then converted to a single-ended output by M11~M14.

Noise analysis (shown in Fig. 2.7.2, where $G_m=2/R_i$) suggests that the noise contribution from output transistors (M11~M14) can be minimized by increasing G_m (reducing R_i), instead of reducing their own aspect ratios. Thus, the proposed LN-OTA eliminates the trade-off between noise performance and voltage headroom mentioned before. In [2], an NEF of 4.0 is achieved by setting the overdrive voltages of the output transistors to 240mV or higher, which allows low aspect ratio. However this is unsuitable for low-voltage rail-rail design. The LN-OTA presented in this paper has achieved a measured NEF of 3.8 while the saturation voltages (V_{Dsat}) of the output transistors are kept below 50mV, enabling rail-rail output under 1V supply. The measured input referred noise is $2.7\mu V_{rms}$ in the signal band from 0.05 to 245Hz with a power dissipation of 330nA at 1V supply voltage. The DC rejection is implemented using pseudo-resistors proposed in [2].

To conserve power, the ADC doesn't have a dedicated S/H circuit. The S/H function is, instead, performed through the output stage of the LN-OTA, which can be considered a pseudo S/H circuit. As shown in Figure 2.7.3, the output of the LN-OTA is connected directly to capacitor array in the successive approximation ADC. During A/D conversion, the two switches (SA and SB) in the output stage of LN-OTA are turned off and the signal is held on the capacitor array in the ADC. After the A/D conversion is completed, SA and SB are turned on. Periodically switching the output stage will introduce error. As illustrated in Fig. 2.7.4, where T_{ADC} represents the period when the amplifier output stage is turned off for A/D conversion and T_{cycle} is the sampling period. According to a first-order model (shown in Fig. 2.7.4, where τ is a constant determined by circuit parameters), if T_{cycle} is sufficiently long and T_{ADC} is sufficiently short, the error caused by switching will be negligible. In this design, the sampling rate is 1kS/s, T_{cycle} is 1ms and T_{ADC} is 2us. The worst case input-referred error for a typical ECG signal is less than ±0.3uV, which is well below the input-referred noise of the LN-OTA and can therefore be ignored.

Conventional capacitor-array-based successive approximation ADC requires a supply voltage higher than $V_{thn}+V_{thp}$ to achieve rail-rail input range. Low-voltage modifications have been reported in [3][4], but [3] lacks rail-rail input range and [4] uses an extra large capacitor to scale down the input voltage prior to conversion. In this design, a modified structure is proposed and shown in Fig. 2.7.3. This structure achieves rail-rail input range as long as the comparator common-mode input range encompasses $V_{DD}/2$. When the ADC is inactive, the output of the LN-OTA is turned on, S1 is switched to V_{DD} and S2~S11 are switched to GND. The node C is charged to V_{in}. During A/D conversion, output stage of the LN-OTA is turned off, the voltage at node C successively approaches $V_{DD}/2$, completing the A/D conversion. The on-chip clock is generated by an 11-stage ring oscillator. Current-steering logic gates are chosen to reduce switching noise. To conserve power, the oscillator is turned on only when the ADC is active. A start-up circuit, as shown in Fig. 2.7.3, is designed to ensure uniform start-up time for every conversion cycle. As an added precaution, the first dozen cycles of the oscillator after start-up are discarded to ensure the quality of the clock for ADC. A dynamic comparator that does not consume any power when inactive is employed to reduce power consumption.

The chip is fabricated in a standard 0.35μm CMOS process ($V_{thp}+V_{thn}$=1.15V). A micrograph of the chip is shown in Fig. 2.7.7. The core area is 1 mm^2 without pads. The measured results are shown in Fig. 2.7.5 and the performance is summarized in Fig. 2.7.6.

References:

[1] M. S. J. Steyaert, W. M. C. Sansen, C. Zhongyuan, "A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes," *IEEE J. Solid State Circuits*, vol. 22, no. 12, pp. 1163–1168, Dec., 1987.

[2] R. R. Harrison, C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid State Circuits*, vol. 38, no. 6, pp. 958-965, June, 2003.

[3] J. Sauerbrey, D. Schmitt-Landsiedel, R. Thewes, "A 0.5V, 1μW Successive Approximation ADC," *Proc. 28th ESSCIRC*, pp. 247-250, Sept., 2002.

[4] T. Yoshida, et al. "A 1V Supply Successive Approximation ADC with Rail-to-Rail Input Voltage Range," *Proc. ISCAS*, pp. 192-195, May, 2005.

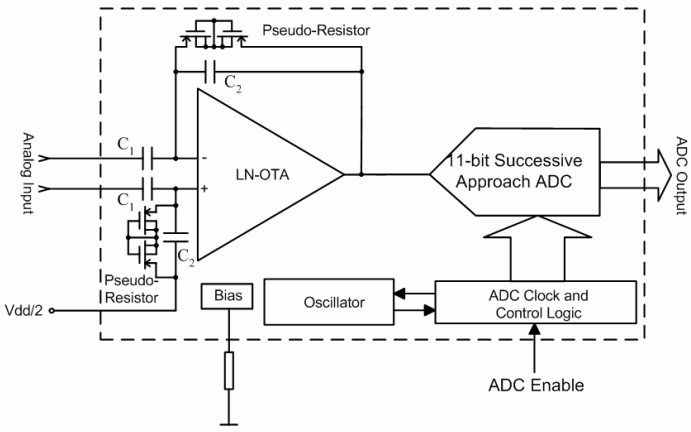
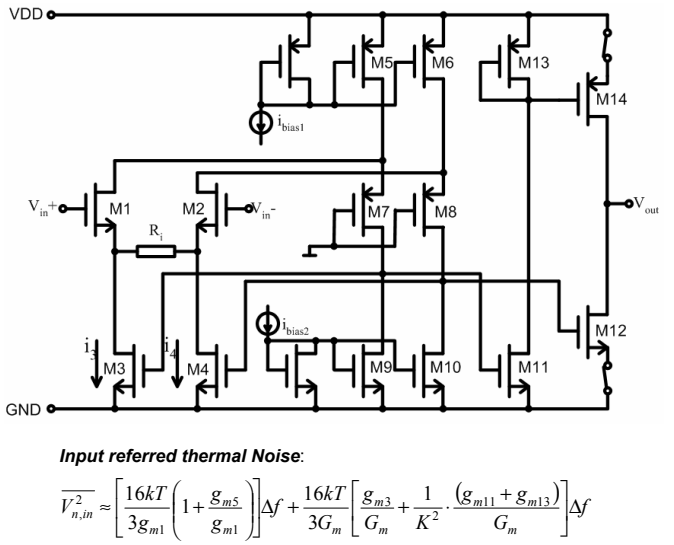


Figure 2.7.1: System block diagram.



Input referred thermal Noise:

$$\overline{V_{n,in}^2} \approx \left[\frac{16kT}{3g_{m1}}\left(1+\frac{g_{m5}}{g_{m1}}\right)\right]\Delta f + \frac{16kT}{3G_m}\left[\frac{g_{m3}}{G_m}+\frac{1}{K^2}\cdot\frac{(g_{m11}+g_{m13})}{G_m}\right]\Delta f$$

Figure 2.7.2: Low-voltage low-power LN-OTA.

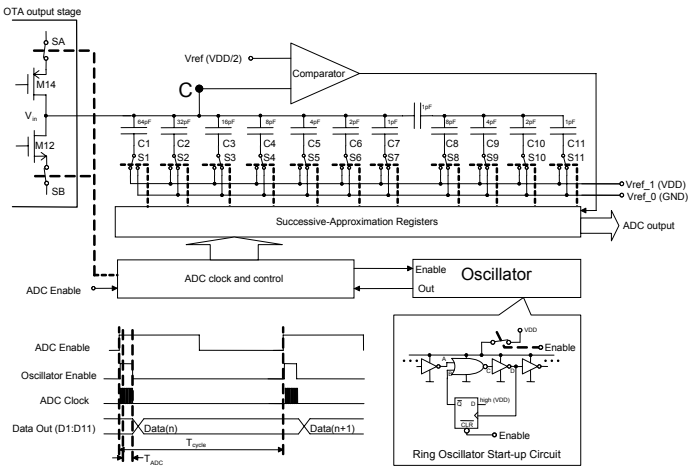


Figure 2.7.3: Pseudo-S/H and modified low-voltage capacitor-array-based ADC.

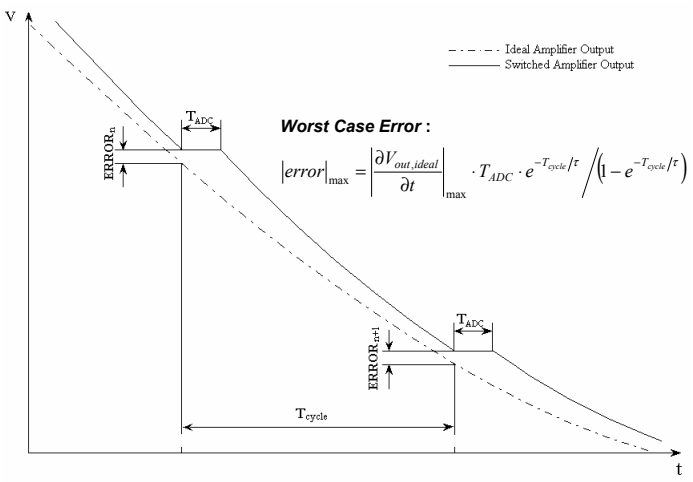


Figure 2.7.4: Error caused by switching (Not drawn to scale for clarity).

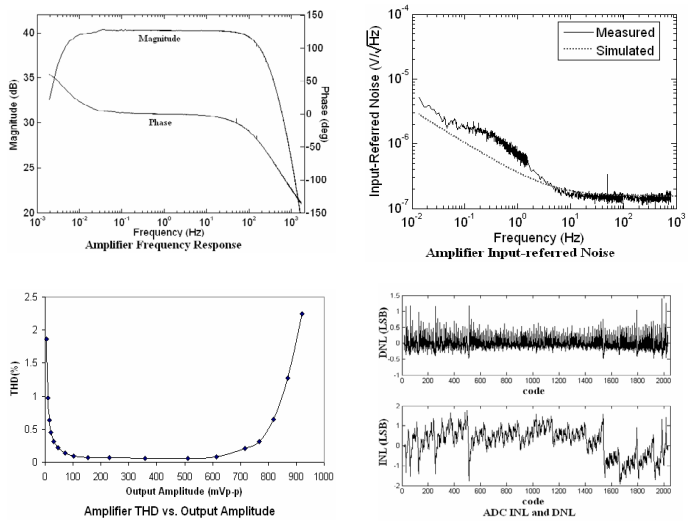


Figure 2.7.5: Measured results.

Measured Performance Summary

Parameter	Remarks	Value
Supply Voltage Range	Parameters measured at 1V	0.8~1.5V
Amplifier current consumption	Bias circuit consumption excluded	330nA
Amplifier Gain	Measured with a 5mVpp 16Hz sine signal	40.2dB
Amplifier 3dB Bandwidth	High-pass / low-pass cutoff	3mHz / 245Hz
Amplifier Input referred noise	Integrated from 0.05Hz to 245Hz	2.7uVrms
Amplifier Noise Efficiency Factor	Bias circuit excluded in NEF calculation	3.8
Amplifier THD	Measured with a 5mVpp 16Hz sine signal	0.053%
Amplifier CMRR	Measured from 1~250Hz, 4 chips	61~64dB
Amplifier PSRR	Measured from 1~250Hz, 4 chips	62~63dB
ADC sampling rate		1kS/s
ADC DNL		< +/- 1.5LSB
ADC INL		< +/- 2LSB
ADC Gain Error		< 1%
Total Current	Bias circuit included	2.3uA
Chip area	Excluding pads	1 mm²

Figure 2.7.6: Measured performance summary.

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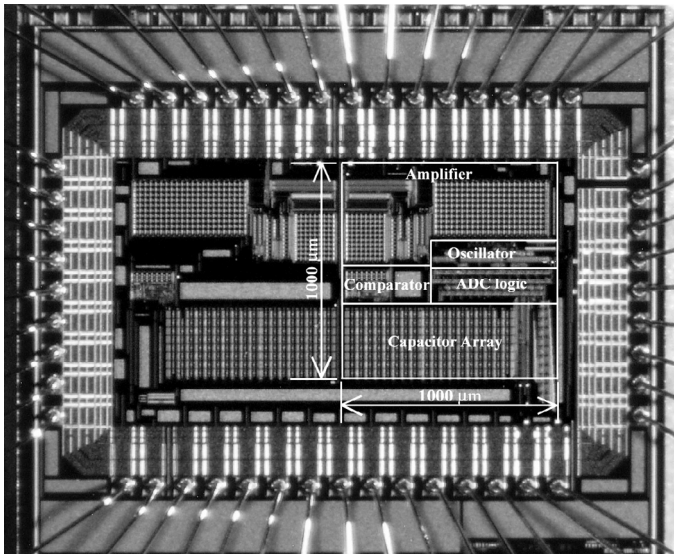

Figure 2.7.7: Die micrograph.

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